IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re **Patent Application:** Dieter E. Staiger et al	**Confirmation No.:** 9027
Application No.: 10/539,111	**Examiner:** Kris M. Rhu
Filed: December 15, 2005	**Group Art Unit:** 2184
Title: "TCET Expander"	

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on **May 26, 2010**.

(**X**) The fee for filing this Appeal Brief is **$540.00** (37 CFR 41.20).

( ) No Additional Fee Required.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provision of 37 CFR 1.136 (a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: CFR 1.17(a)-(d)) for the total number of months checked below:

( )	one month	$130.00
( )	two months	$490.00
( )	three months	$1110.00
( )	four months	$1730.00

( ) The extension fee has already been filed in this application

(**X**) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant had inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 09-0461/ DE920020033US1 the sum of $540.00. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 09-0461/ DE920020033US1 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 09-0461/ DE920020033US1 under CFR 1.16 through 1.21 inclusive, and any other section in the Title 37 of the Code of Federal Regulations that may regulate fees.

Respectfully submitted,

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Date: July 1, 2010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Patent Application of Dieter E. Staiger et al.	Group Art Unit: 2184
Application No. 10/539,111	Examiner: Kris M. Rhu
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For: TCET Expander	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal Brief under Rule 41.37 appealing the decision of the Primary Examiner dated March 26, 2010 (the "final Office Action" or "Action"). Each of the topics required by Rule 41.37 is presented herewith and is labeled appropriately.

I. Real Party in Interest

The inventors have assigned their interests in the present application to International Business Machines Corporation ("IBM"), which has a principal place of business at New Orchard Road, Armonk, NY 10504. Accordingly, the real party in interest is IBM.

II. Related Appeals and Interferences

There are no appeals or interferences related to the present application of which the Appellant is aware.

III. Status of Claims

No claims have been cancelled.

Claims 1-10 are currently pending in the application and stand finally rejected.

Accordingly, Appellant appeals from the final rejection of claims 1-10, which claims are presented in the Appendix.

IV. Status of Amendments

No amendments have been filed subsequent to the Office Action of March 26, 2010, from which Appellant takes this appeal.

V. Summary of Claimed Subject Matter

A summary is given below of the subject matter defined in each of the independent claims at appeal and the subject matter defined in any claim at appeal reciting a "means plus function" clause in accordance with the requirements of 35 C.F.R. § 41.37(c)(1)(v). The citation to passages in the specification and drawings for each claim element does not imply that the limitations from the cited passages in the specification and drawings should be read into the corresponding claim elements. *See Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875, 69 USPQ2d 1865, 1868 (Fed. Cir. 2004); M.P.E.P. § 2111.01(II). Citations to one or more line numbers in connection with a specific paragraph refer to the lines within that paragraph, and not necessarily to the lines in the page where that paragraph appears.

Turning to Appellant's specific claims,

Claim 1 recites:

A circuit in an embedded processing system covering a number of technical applications, a number of operative functions of the number of technical applications being performed via a respective number of application-specific Electronic Control Units (ECU), the circuit comprising:

a) a number of controller means (30A-E, Figs. 2-3, secondary layer 60, Figs. 4-5) for controlling respective application specific ECUs, each of the controller means (30A-E, Figs. 2-3) comprising a number of application-specific support functions and I/O subsystems (*e.g.*, Appellant's Specification, p. 4 lines 5-25, p. 8 lines 10-24, p. 9 lines 4-8, p. 10 lines 10-15, p. 11 line 25 to p. 12 line 1); and

b) a number of processor units (40, Figs. 2-5) each having an I/O-interface operatively connecting to a respective one of the controller means (30A-E, Figs. 2-3, secondary layer 60, Figs. 4-5) and supplying that controller means (30A-E, Figs. 2-3, secondary layer 60, Figs. 4-5) with computing power (*e.g.*, Appellant's Specification, p. 4 lines 4-24, p. 8 lines 3-8, p. 9 lines 4-18, p. 9 line 25 to p. 10 line 8);

wherein at least one of the processor units (40, Figs. 2-5) and a respective controller means (30A-E, Figs. 2-3, secondary layer 60, Figs. 4-5) are implemented on different chips (*e.g.*, Appellant's Specification, p. 4 lines 14-25, p. 7 line 30 to p. 8 line 24, Figs. 2-3).

Claim 2 recites:

The circuit according to claim 1, further comprising mapping means (mapping electronic circuit 26, Fig. 3, broker and arbitration layer 70, Figs. 4-5) for mapping the I/O subsystems to the processor units (*e.g.*, Appellant's Specification, p. 9 lines 4-18, p. 10 lines 17-21) and a General Controller Unit (12, Figs. 3-5) operatively coupled to the mapping means (mapping electronic circuit 26, Fig. 3, broker and arbitration layer 70, Figs. 4-5) and configured to dynamically switch at least one of the processor units (40) into communication with a selected controller means (30A-E, Figs. 2-3, secondary layer 60, Figs. 4-5) based on processor timing requirements (*e.g.*, Appellant's Specification, p. 4 line 27 to p. 5 line 2).

Claim 3 recites:

The circuit according to claim 2, further comprising:

a primary layer (50, Figs. 4-5) comprising basic configuration layout data and an interface means for connecting to the number of processor units (40) (*e.g.*, Appellant's Specification, p. 5 lines 4-18, p. 9 line 30 to p. 10 line 8, p. 11 lines 4-23, Figs. 4-5); and

a secondary layer (60) comprising a preprogrammed, autonomic state switching means (62), a preprogrammed emergency switching means (64), and a port interface means (66) connected to at least one of the I/O subsystems (*e.g.*, Appellant's Specification, p. 5 lines 4-18, p. 10 lines 10-15, p. 11 line 25 to p. 12 line 27, Figs. 4-5).

Claim 4 recites:

The circuit according to claim 3, further comprising an additional controller operatively coupled to the General Controller Unit (12, Figs. 3-5) and configured to implement a monitoring function for monitoring the operational status of the processor units (40) and the controller means (30A-E, Figs. 2-3, secondary layer 60, Figs. 4-5) (*e.g.*, Appellant's Specification, p. 5 lines 20-27).

Claim 8 recites:

A method of operating an embedded processing system comprising:

controlling a number of electronic control units with a number of interface expander controllers (30A-E, Figs. 2-3, secondary layer 60, Figs. 4-5), wherein said interface expander controllers (30A-E, Figs. 2-3, secondary layer 60, Figs. 4-5) are disposed on a separate chip from said electronic control units (*e.g.*, Appellant's Specification, p. 4 lines 14-25, p. 7 line 30 to p. 8 line 24, Figs. 2-3); and

providing computing power to said interface expander controllers (30A-E, Figs. 2-3, secondary layer 60, Figs. 4-5) with a separate number of processors (40) (*e.g.*, Appellant's Specification, p. 4 lines 14-25, p. 7 line 30 to p. 8 line 24, Figs. 2-3).

VI. Grounds of Rejection to be Reviewed on Appeal

The Office Action raised the following grounds of rejection.

(1) Claims 1-4 and 7-10 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent Application No. 2004/0205386 by Staiger ("Staiger").

(2) Claim 5 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Staiger taken alone.

(3) Claim 6 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Staiger in view of U.S. Patent No. 6,579,231 to Phipps ("Phipps").

Accordingly, Appellant hereby requests review of each of these grounds of rejection in the present appeal.

VII. Argument

(1) Claims 1-4 and 7-10 are patentable over Staiger:

Claims 1-4 and 7-10 stand rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Staiger. For at least the following reasons, this rejection is respectfully traversed and should not be sustained.

The present application is a national stage application filed under 35 U.S.C. § 371 for PCT International Application No. 03/12167, which claims priority from European Patent Office Application No. 02102830.3 (filed December 2, 2002). The present application entered the PCT stage on October 31, 2003, and the U.S. national stage on December 15, 2005.

According to M.P.E.P. § 1893.03(b) expressly states that

> [a]n international application designating the U.S. has two stages (international and national) with the filing date being the same in both stages. Often the date of entry into the national stage is confused with the filing date. It should be borne in mind that the filing date of the international stage application is also the filing date for the national stage application.

See also 35 U.S.C. § 363; PCT Art. 11(3). Thus, under these requirements, "the date of the application for patent in the United States" from which the one-year anticipation bar to patentability of 35 U.S.C. § 102(b) is measured for the present application is the international filing date. M.P.E.P. § 706.02(VI) confirms that the effective filing date for a national stage application filed under 35 U.S.C. § 371 is determined by M.P.E.P. § 1893.03(b) for the purposes of a prior art rejection.

Furthermore, Article 4 of the Paris Convention for the Protection of Industrial Property ("Paris Convention") expressly states that "[a]ny filing that is equivalent to a regular national filing under the domestic legislation of any country of the Union or under bilateral or

multilateral treaties concluded between countries of the Union shall be recognized as giving rise to the right of priority." Paris Convention, Art. 4 §§ A, C. The Patent Cooperation Treaty incorporates this provision of the Paris Convention to international applications. Patent Cooperation Treaty, Art. 8. Thus, because the present application is the U.S. national stage of an international application which properly claims priority from a national stage application filed in the European Patent Office, the effective international filing date of the present application is the filing date of the original European Patent Office Application, December 2, 2002.

Thus, only references that were published more than one year prior to the "date of the application for patent in the United States" qualify as prior art against a patent application under 35 U.S.C. §§ 102(b) and 119(a). Because the effective "date of the application for patent in the United States" for the present application is the filing date of the original European Patent Office Application, a reference cannot be applied as prior art against the present application under 35 U.S.C. § 102(b) unless that reference was published prior to December 2, 2001. *See* 35 U.S.C. §§ 102(b), 119(a), 363; Patent Cooperation Treaty Art. 11(3); Paris Convention, Art. 4 §§ A,C; M.P.E.P. §§ 1893.03(b); 706.02(VI).

The Staiger reference was filed in this country on March 16, 2004 and was first published on October 14, 2004. No publication of the Staiger reference or its European parent application (EP03100780.0) occurred in any country prior to the October 14, 2004 U.S. publication. October 14, 2004 indisputably occurred after December 2, 2001. Consequently, the Staiger reference was not published prior to one year before the effective filing date of the present application, and therefore cannot qualify as prior art against the present application under 35 U.S.C. § 102(b).

The final Office Action cites to M.P.E.P. § 706.02(VI)(C) which notes that if an application claims foreign priority under 35 U.S.C. §§ 119(a)-(d) or 365(a) or (b), the effective filing date is the filing date of the U.S. application, unless certain situations apply, and that [t]he filing date of the foreign priority document is not the effective filing date." (Action, pp. 9-10). Nevertheless, the assertion that this statement applies to the present application fails on multiple grounds.

First, this statement of the M.P.E.P. applies only to applications filed as separate national applications under 35 U.S.C. §§ 119(a)-(d) or 365(a) or (b). However, the present application was not filed under any of these sections; rather, the present application was filed as the national stage of an international application under 35 U.S.C. § 371. As mentioned above, the M.P.E.P. is quite clear that the effective international filing date of such applications is the effective U.S. filing date. M.P.E.P. §§ 706.02(VI), 1893.03(b).

Additionally, it appears that the Examiner has failed to understand that the "filing date of the U.S. application" in the instant case is the effective international filing date of December 2, 2002, which predates any publication of the Staiger reference. Thus, even if the condition in the M.P.E.P. cited by the Examiner did apply to the present application, the effective filing date of the present application would still disqualify the Staiger reference as prior art under 35 U.S.C. § 102.

Appellant notes that "[t]he examiner bears the initial burden . . . of presenting a *prima facie* case of unpatentability." *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Because the present rejection of claims 1-4 and 7-10 relies entirely on a reference that cannot be applied as prior art against the present application, the Office has failed to meet its burden to establish the *prima facie* unpatentability of these claims. For at least these reasons, the rejection of claims 1-4 and 7-10 should not be sustained.

(2) Claim 5 is patentable over Staiger:

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Staiger taken alone. This rejection is respectfully traversed and should not be sustained for at least the same reasons given above in favor of the patentability of independent claim 1. *See In re Fine*, 837 F.2d 1071, 1076, 5 USPQ2d 1596 (Fed. Cir. 1988) (if an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

Moreover, the office may reject a claim under 35 U.S.C. § 103(a) only if the prior art references relied upon by the office in making the rejection qualify as prior art against the claim under 35 U.S.C. § 102. *See* 35 U.S.C. § 103(a). As demonstrated above, the Staiger reference does not qualify as prior art against the present application under 35 U.S.C. § 102. Consequently, the Staiger reference cannot qualify as prior art against claim 5 under 35 U.S.C. § 103(a). For at least these reasons, the Office has failed to meet its burden to establish the *prima facie* unpatentability of claim 5. Therefore, the rejection of claim 5 should not be sustained.

(3) Claim 6 is patentable over Staiger and Phipps:

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being allegedly obvious over Staiger in view of Phipps. This rejection is respectfully traversed and should not be sustained for at least the same reasons given above in favor of the patentability of independent claim 1. *See In re Fine*, 837 F.2d 1071, 1076, 5 USPQ2d 1596 (Fed. Cir. 1988) (if an independent claim is nonobvious, then any claim depending therefrom is nonobvious); M.P.E.P. § 2143.03.

Moreover, as demonstrated above with respect to the rejection of claims 1 and 5, Staiger does not qualify as a prior art reference against claim 6. For at least these reasons, the

Office has not met its burden to establish the *prima facie* unpatentability of claim 6. Therefore, the rejection of claim 6 should not be sustained.

In view of the foregoing, it is submitted that the final rejection of the pending claims is improper and should not be sustained. Therefore, a reversal of the Rejection of March 26, 2010 is respectfully requested.

Respectfully submitted,

DATE: July 1, 2010

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VIII. CLAIMS APPENDIX

1. (previously presented) A circuit in an embedded processing system covering a number of technical applications, a number of operative functions of the number of technical applications being performed via a respective number of application-specific Electronic Control Units (ECU), the circuit comprising:

a) a number of controller means for controlling respective application specific ECUs, each of the controller means comprising a number of application-specific support functions and I/O subsystems; and

b) a number of processor units each having an I/O-interface operatively connecting to a respective one of the controller means and supplying that controller means with computing power,

wherein at least one of the processor units and a respective controller means are implemented on different chips.

2. (previously presented) The circuit according to claim 1, further comprising mapping means for mapping the I/O subsystems to the processor units, and a General Controller Unit operatively coupled to the mapping means and configured to dynamically switch at least one of the processor units into communication with a selected controller means based on processor timing requirements.

3. (previously presented) The circuit according to claim 2, further comprising:

a primary layer comprising basic configuration layout data and an interface means for connecting to the number of processor units; and

a secondary layer comprising a preprogrammed, autonomic state switching means, a preprogrammed emergency switching means, and a port interface means connected to at least one of the I/O subsystems.

4. (previously presented) The circuit according to claim 3, further comprising an additional controller operatively coupled to the General Controller Unit and configured to implement a monitoring function for monitoring the operational status of the processor units and the controller means.

5. (previously presented) The circuit according to claim 1, further comprising a database storing instructions on how to handle specific errors associated with the number of processor units.

6. (previously presented) The circuit according to claim 1, further comprising a number of emergency controllers for continuously storing current global positioning system (GPS) coordinates and configured to send an emergency signal including the coordinates in case a number of external sensor devices detect an emergency case.

7. (previously presented) An embedded system having an electronic circuit according to claim 1.

8. (previously presented) A method of operating an embedded processing system comprising:

controlling a number of electronic control units with a number of interface expander controllers, wherein said interface expander controllers are disposed on a separate chip from said electronic control units; and

providing computing power to said interface expander controllers with a separate number of processors.

9. (previously presented) The method of claim 8, further comprising selectively providing communication between said interface expander controllers and said processors with a General Controller Unit.

10. (previously presented) The method of claim 8, further comprising disposing said interface expander controllers on a single Application Specific Integrated Circuit.

IX. Evidence Appendix

None

X. Related Proceedings Appendix

None

XI. Certificate of Service

None